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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

RICHARD W. ARNOLD ET AL.

Serial No. 09/164,580 (ti-22561)

Filed October 1, 1998

For: KNOWN GGOD DIE USING EXISTING PROCESS INFRASTRUCTURE

Art Unit 2827

Examiner James M. Mitchell

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9-10-04

Jay M. Cantor, Reg. No. 19,906

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences.

STATUS OF CLAIMS

This is an appeal of claims 9, 10, 13, 14 and 22 to 31, all of the rejected claims. Claims 1 to 4 have been allowed, the non-elected claims 17 to 21 are the subject of Serial No. 09/986,341 which has been allowed. Claims 22 to 31 have been copied from Patent No.

6,028,437 for purposes of having an interference declared. Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

An amendment was not filed after a second or subsequent rejection, this being a second reopening of prosecution after filing of a Notice of Appeal and a Brief on Appeal..

SUMMARY OF INVENTION

The invention relates to an apparatus adaptable for the testing of semiconductor devices which includes a package (110 of Fig. 1) and an interconnecting medium (140) contained within the package and having electrical paths (171-173) adaptable for coupling to test circuitry. The interconnecting medium (140) includes a medium surface (to surface of 140 in Fig. 1b), a plurality of standoffs (13 of Fig. 3) affixed to the medium surface and a plurality of compliant probe tips (11 of Fig. 3) affixed to the medium surface, the probe tips being adaptable for making electrical contact with pads on the semiconductor device.

The interconnecting medium or layer for use in a semiconductor package includes an electrically insulating layer (140), electrically conductive paths on the layer (171 to 173), each of the paths having first and second spaced apart regions thereon, the second spaced apart region of each of the paths having a compliant bump (11) having a height greater than all other structures on the layer. A standoff (13) is disposed on the layer and has a height above the layer and less than the bump. The package (110) further includes a package base having an upper surface (base of cavity 112) adapted to receive the interconnecting medium (140), the medium having a medium lower surface (lower surface of 140). A bonding layer (120 and 135), preferably comprised of an elastomeric material, is interposed between the

medium lower surface and the package base upper surface and a package base upper surface and a package lid (160) is provided having a lower surface adapted to receive the semiconductor device, the package lid positioned above the package base. The semiconductor device, the package lid positioned above the package base. The semiconductor device is a die (130) having an upper surface fixed to the package lid lower surface by a bonding layer interposed therebetween (140 and 150). The bonding layer interposed between the die and the package lid lower surface is comprised of an elastomeric material (page 9, line 11). The compliant bump probe tips are comprised of a solid material (see, for example, Patent No. 5,508,228 cited at page 11, line 15).

ISSUES

The issues on appeal are as follows:

1. Whether claims 9, 10, 13 and 14 are anticipated by Knight et al. (U.S. 6,728,113) under 35 U.S.C. 102(e).

2. Whether claim 22 to 31 are anticipated by Potter (U.S. 6,028,437) under 35 U.S.C. 102(b).

GROUPING OF CLAIMS

The claims do not stand or fall together for reasons set forth hereinbelow under ARGUMENT.

ARGUMENT

ISSUE 1

Claims 9, 10, 13 and 14 were rejected as being anticipated by Knight et al. (U.S. 6,728,113) under 35 U.S.C. 102(e). The rejection is without merit.

Claim 9 relates to an interconnecting layer for use in a semiconductor package and includes, among other features, an electrically insulating layer, electrically conductive paths on the layer, each path having first and second spaced apart regions thereon, the second spaced apart region of each path having a compliant bump having a height greater than all other structures on the layer. No such feature is taught by Knight et al. The examiner alleges that compliant bumps are shown in Knight et al. at column 20, lines 22 to 28. This is clearly not the case. The section of Knight et al. referred to discusses conductive connections which are not numbered and it is not clear what these are from the specification or drawing. Accordingly, for this reason alone, there is no basis to ascribe the structure and function to these unnumbered elements which also possibly not shown in the figures. More importantly, there are no compliant bumps shown in Knight et al. even assuming that compliant contacts appear somewhere in Knight et al. Still further, there are no compliant bumps in Knight et al. which have a height greater than all other structures on the layer, as claimed.

Claim 9 further requires a standoff disposed on the layer and having a height above the layer and less than the bump. No such structure is taught by Knight et al. The examiner alleges that "'spacers', not shown , Col. 16, Lines 59-60" correspond to the standoffs. There is no basis whatsoever for this allegation and there is nothing in the cited section of Knight et al. to in any way suggest that there is a disclosure of a standoff disposed on the layer and having a height above the layer and less than the bump. In fact, there isn't even a correlation in Knight et al. between what the examiner alleges is the bump of Knight et al. and what the examiner alleges is the standoff of Knight et al., let alone that correlation as set forth in the claim.

Claims 10, 13 and 14 depend from claim 9 and therefore define patentably over Knight et al. for at least the reasons set forth above with reference to claim 9.

Claim 10 further limits claim 9 by requiring that the second region be a bump extending above the level of the electrically conductive path. No such feature is taught by Knight et al. either alone or in the combination as claimed for reasons as stated above with reference to claim 9.

ISSUE 2

Claim 22 to 31 were rejected as being anticipated by Potter (U.S. 6,028,437) under 35 U.S.C. 102(b). The rejection is without merit.

Claims 22 to 31 were copied from Potter (U.S. 6,028,437) for purposes of interference. On November 15, 2001, a Declaration Under 37 C.F.R. 1.131 was filed by the appellants herein swearing back of the filing date of Potter. It follows that the examiner must act in one of several manners.

To begin with, the examiner must determine whether the claims copied from Potter can be made in the subject application. In this regard, appellants demonstrated in minute detail how the claims of Potter were readable on the subject disclosure in the prior filed Briefs on Appeal as well as in REMARKS in amendments and this has not been challenged. It must therefore be assumed that this is not as issue herein.

Once ability to make claims or a proper count has been established, which is the case herein, the examiner must consider the Declaration Under 37 C.F.R. 1.131 to determine whether the claimed invention or count is established in that Declaration. This has also not been challenged, so it must be assumed that the Declaration establishes a date of conception with diligence as well as reduction to practice prior to the filing date of Potter et al. In

addition, the Declaration establishes a date of "invention" prior to the filing date of Potter as established in the decision by the United States Supreme Court in Pfaff v. Wells Electronics, 525 U.S. 55 (U.S. 1998).

Since it has been established that appellants herein can make the claims of Potter and antedate the filing date of Potter, a rejection under 35 U.S.C. 102 is improper. The Examiner must either have an interference established as requested or determine that the claims copied from Potter and not patentable to appellants. The latter has not been done. Accordingly, the rejection is improper, should be reversed, and an interference declared as requested about three years ago.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,

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APPENDIX

The claims on appeal read as follows:

9. An interconnecting layer for use in a semiconductor package which comprises;

(a) an electrically insulating layer;

(b) electrically conductive paths on said layer, each of said paths having first and second spaced apart regions thereon, said second spaced apart region of each of said paths having a compliant bump having a height greater than all other structures on said layer; and

(c) a standoff disposed on said layer and having a height above said layer and less than said bump.

10. The layer of claim 9 wherein said second region is a bump extending above the level of said electrically conductive path.

13. The layer of claim 9 wherein said layer is flexible.

14. The layer of claim 10 wherein said layer is flexible.

22. An apparatus adaptable for the testing of semiconductor devices comprising:

a package; and

an interconnecting medium contained within said package having electrical paths adaptable for coupling to test circuitry, wherein said interconnecting medium includes a medium surface, a plurality of standoffs affixed to said medium surface, and a plurality of probe tips affixed to said medium surface, said probe tips adaptable for making electrical

contact with pads on said semiconductor device, wherein said probe tips are compliant bump probe tips.

23. The apparatus of claim 22, said package further comprising:

a package base having an upper surface adapted to receive said interconnecting medium, said medium having a medium lower surface;

a bonding layer interposed between said medium lower surface and said package base upper surface; and

a package lid having a lower surface adapted to receive said semiconductor device, wherein said package lid is positioned above said package base.

24. The apparatus of claim 23, wherein said bonding layer is comprised of an elastomeric material.

25. The apparatus of claim 23, wherein said semiconductor device is a die having an upper surface, said upper surface fixed to said package lid lower surface by a bonding layer interposed therebetween.

26. The apparatus of claim 23, wherein said semiconductor device is a wafer having an upper surface, said upper surface fixed to said package lid lower surface by a bonding layer interposed therebetween.

27. The apparatus of claim 4, wherein said bonding layer interposed between said die and said package lid lower surface is comprised of an elastomeric material.

28. The apparatus of claim 5, wherein said bonding layer interposed between said wafer and said package lid lower surface is comprised of an elastomeric material.

29. The apparatus of claim 22, wherein the compliant bump probe tips are comprised of a solid material.

30. An apparatus adaptable for the testing of semiconductor devices comprising:

a package, wherein said package has a package lid having a lower surface adapted for receiving said semiconductor device, said semiconductor device having an upper surface, and a package base having an upper surface;

an interconnecting medium contained within said package, wherein said interconnecting medium has electrical paths adaptable for coupling to test circuitry, said medium including a medium surface, said medium surface having a plurality of probe tips affixed thereto, a plurality of standoffs affixed thereto, and a lower surface, wherein said probe tips are adaptable for making electrical contact with pads on said semiconductor device and are compliant bump probe tips;

a bonding layer comprising an elastomeric material interposed between said package lid lower surface and said semiconductor device upper surface; and

a bond layer comprising an elastomeric material interposed between said interconnecting medium lower surface and said package base upper surface, said package base being adapted for receiving said interconnecting medium.

31. The apparatus of claim 30, wherein the compliant bump probe tips are comprised of a solid material.